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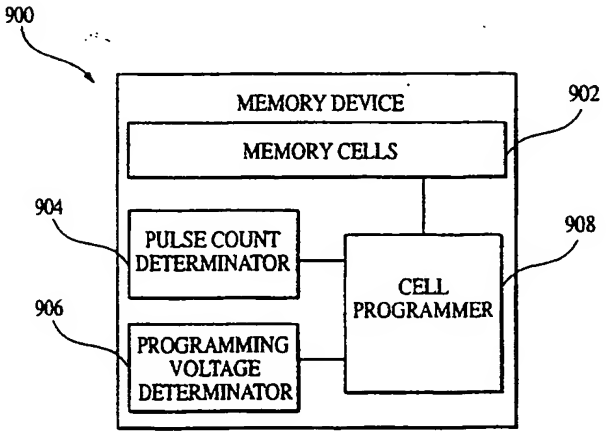
(54) Title: MULTILEVEL CELL PROGRAMMING



(57) Abstract: Method of storing and retrieving multiple bits of information in a multi-level cell (902) of non-volatile memory (900) including programming a plurality of multi-level memory cells (902) within a programming time target. The multi-level memory cells (902) having at least first, second, third and fourth programming levels. The fourth programming level being the erase state, the first programming level being the programming level furthest from the fourth programming level. The second and third programming levels being within the first and fourth programming levels, includes erasing the plurality of multi-level memory cells (902). Then, programming a first group of multi-level memory cells (902) with the first programming level with a first programming pulse count having a first pulse width and a first programming voltage. Then, programming a second group of multi-level memory cells (902) with the second programming level with a second programming pulse count having a second pulse width and a second programming voltage. Then programming a third group of multi-level memory cells (902) with the third programming level with a third programming pulse count having a third pulse width and a third programming voltage.

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MULTILEVEL CELL PROGRAMMING

BACKGROUND ART

A flash memory cell can be a field effect transistor (FET) that includes a select gate, a floating gate, a drain, and a source. A memory cell can be read by grounding the source, and applying a voltage to a bitline connected with the drain. By applying a voltage to the wordline connected to select gate, the cell can be switched on and off.

Programming a memory cell includes trapping excess electrons in the floating gate to increase voltage. This reduces the current conducted by the memory cell when the select voltage is applied to the select gate. The memory cell is programmed when the memory cell current is less than a reference current and the select voltage is applied. The memory cell is erased when the memory cell current is greater than the reference current and the select voltage is applied.

Memory cells with only two programmable states contain only a single bit of information, such as a "0" or a "1".

A multi-level cell ("MLC") can be programmed with more than one voltage level. Each voltage level is mapped to corresponding bits of information. For example, a multi-level cell is programmed with one of four voltage levels, -2.5V, 0.0V, +1.0V, +2.0V that correspond to binary "00", "01", "10", and "11", respectively. A cell that is programmable at more voltage levels can store more bits of data based on the following equation:

$N = 2^B$ Eqn. 1

B is the number of bits of data stored

N is the number of voltage levels.

Thus, a 1 bit cell requires 2 voltage levels, a 2 bit cell requires 4 voltage levels, a 3 bit cell requires 8 voltage levels, and a 4 bit cell requires 16 voltage levels.

Two of the primary data reliability issues for memory cells, particularly NAND flash, are the "data retention" effect and "read disturb" effect. The "data retention" effect is a shift in voltage that results from the normal passage of time. This shift is toward the erase state. The "read disturb" effect is a shift in the voltage that results from reading the memory cell. For the read disturb effect to be appreciable, many reads must occur. The read disturb effect and the data retention effect shift the voltage in opposite directions.

When the voltage level shifts too far in either direction, it will be interpreted as representing the next higher or lower voltage level and thus the data will be misread. To prevent such misreads, the "data retention" effect and "read disturb" effect should be optimized to minimize the voltage shifts.

Figure 1 shows a representation of a four level multilevel cell program voltage diagram 100. The program voltage distribution ("distribution") of the four levels are shown between lines 102 and 104, 106 and 108, lines 110 and 112, and above line 114, respectively. The programming distribution can be for example 100mV to 600mV wide. A four level multilevel memory cell can be programmed with any one of these voltage levels. Because the cell can store one of four binary values it can store 2 bits of information. The data margin ("margin"), also called a guard band, is the voltage levels between distributions that is not normally used. The margins are shown in Figure 1 between lines 104 and 106; lines 108 and 110; and lines 112 and 114. For example, the data margin can be 800mV to 100mV wide.

Figure 2 shows the affect of the phenomena called "read disturb." Read disturb occurs after the cell has been read many times without being reprogrammed. The programming distributions are shifted to the right, which represents a positive voltage shift. Distributions 230, 232, 234, and 236 represent the distributions 220, 222, 224, and 226 after they have been affected by the read disturb. Eventually, the read disturb can become so severe that the stored data becomes unreliable, such as at lines 210 and 212.

Figure 3 shows the affect of the phenomena called "data retention." Data retention causes the distributions 220, 222, 224, and 226 to be shifted to the left as shown by distributions 320, 322, 324, and 326, which represents a negative voltage shift. Over time if the cell is not reprogrammed, the data retention shift can cause the stored data to become unreliable.

DISCLOSURE OF THE INVENTION

Method of storing and retrieving multiple bits of information in a multi-level cell of non-volatile memory including programming a plurality of multi-level memory cells within a programming time target. The multi-level memory cells having at least first, second, third and fourth programming levels. The fourth programming level being the erase state, the first programming level being the programming level furthest from the fourth programming level. The second and third programming levels being within the first and fourth programming levels, includes erasing the plurality of multi-level memory cells. Then, programming a first group of multi-level memory cells with the first programming level with a first programming pulse count having a first pulse width and a first programming voltage. Then, programming a second group of multi-level memory cells with the second programming level with a second programming pulse count having a second pulse width and a second programming voltage. Then programming a third group of multi-level memory cells with the third programming level with a third programming pulse count having a third pulse width and a third programming voltage.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention is illustrated by way of example and not limitation in the accompanying figures. In the figures, like reference numbers indicate identical or functionally similar elements. Additionally, the left-most digit(s) of a reference number identifies the figure in which the reference number first appears.

Figure 1 is a representation of the programmable voltage levels of a multi-level cell;

Figure 2 is a representation of the programmable voltage levels of a multi-level cell with a positive voltage shift;

Figure 3 is a representation of the programmable voltage levels of a multi-level cell with a negative voltage shift;

Figure 4 is a representation of narrower programmable voltage levels of a multi-level cell with a positive voltage shift;

Figure 5 is a representation of wider programmable voltage levels of a multi-level cell with a positive voltage shift;

Figure 6 is a representation of the voltage margin per pulse count;

Figure 7 is a representation of the programmable voltage levels of a multi-level cell with distributions created by 5 and 10 pulses; and

Figure 8 is a flow diagram of an embodiment of the multilevel cell programming method; and

Figure 9 is a diagram of a memory device.

MODES OF CARRYING OUT THE INVENTION

Multi-bit memory cell programming can be optimized by programming cells based on the value to be stored rather than traditional serial programming. Because the voltage level and programming pulse count vary depending on which value is stored in a memory cell, traditional serial programming requires time to adjust for each memory cell. An example of an embodiment of the present invention applied to a two-bit memory cell is: programming all the memory cells that will have the binary value of "11", then programming the memory cells that will have the binary value of "10", then programming the memory cells that will have the binary value of "01." This is done on a page by page basis. A page typically has 1024 cells. The value of "00" does not need to be programmed because it is equivalent to the erase state. In this embodiment, the programming circuit will have to adjust the programming level and pulse count only three times rather than 1024 times.

Because the voltage levels of the stored data can shift to the left or the right as shown in Figures 2 and 3, it is beneficial to have narrower program distributions and thus wider program margins. Figures 4 and 5 illustrate this. Figure 4 has program distributions of approximately 200mV, while Figure 5 has program distributions of 400mV. If the program distributions 404 and 504 in Figure 4 and 5 respectfully are shifted to the right by 100mVs, the data distribution 406 in Figure 4 will still be read properly at read point 402, while the data distribution 506 in Figure 5 will be read incorrectly at read point 502. The read points 402 and 502 represent the threshold voltage value that separate the zero volt distribution from the one volt distributions. That is, if the voltage is above the read point the cell is read as the two bits associated with the one volt distribution and if the read voltage is below the read point then the cell is read as the two bits associated with the zero volt distribution.

While the narrower program distributions of Figure 4 are more reliable than those of Figure 5, to achieve the narrower program distributions require longer programming time. Programming time is the time required to program a cell to a voltage within a valid program distribution. A cell is programmed by applying one or more pulses at a voltage level. The voltage level of the pulses is often much higher then the voltage distribution. For example, to program a cell to the one volt distribution, 2 pulses at 20V can be used. However, to achieve a narrower program distribution, 20 pulses at 16V may be used. Thus, a fundamental trade off is made between programming speed and program margin.

Figure 6 shows the relation of the programming pulse count to the data margin for a multilevel NAND flash cell. The maximum data margin is represented by line 606 and occurs between thirty and forty pulses. The data margin falls off slightly after forty pulses because of program disturb. Line 606 represents a data margin of approximately 940mV, which is the maximum data margin. At line 602 ten pulses have programmed the cell to approximately 85% of the maximum data margin, approximately 800mV. At line 604 twenty pulses have programmed the cell to approximately 95% of the maximum data margin, approximately 895mV. The 85% and 95% points are significant, regardless of the memory cell type, for determining how many pulses should be used for optimizing between programming time and data margin.

Narrower program distributions can be accomplished by programming the cell with a series of pulses. The greater the number of pulses used to program the cell, the narrower the program distributions. However, as

the number of pulses used to program a cell increases, the time required to program the cell also increases according to the following equation:

Program Time = Pulses x (Pulse width + Verify time) Eqn. 2

For example, if 20 pulses with a width of 10 microseconds are used to program the cell, and a 4 microsecond verify time is requires, the time required to program the cell is 280 microseconds, (20 x 10microseconds + 20 x 4microseconds).

Figure 7 shows a diagram of programmable voltage levels of a multi-level cell. The 1V program distribution 702 and the 2V program distribution 704 both correlate to programming with 10 pulses while the 2v program distribution 706 correlates to programming with only 5 pulses. The program distribution 706 (5 pulses) is shorted and wider than the program distribution 704 (20 pulses). Thus, the program distribution correlates positively with the pulse count and is not related to the program time. Thus, a cell that is programmed with twenty 18.0V pulses with 10 microsecond pulse width can have the same or similar program distribution as a cell that is programmed with twenty 18.5V pulses with 5 microsecond pulse width. However, the first cell would have a program time of 280 microseconds and the second cell would have a program time of only 180 microseconds.

In Figure 8, a method 800 determines the optimal programming of a multi-level cell.

In 802, the maximum total programming time allowable is identified. This is the total time for programming all the cells at the three program distributions. For example, target program time is 300 microsecond. The fourth voltage level is the erase state, for example -2.5V, and does not need to be programmed because the page was erase before being programmed.

In 804, the desired pulse count for the middle program distributions is identified. For example the zero volt and one volt program distributions. From Figure 6, a pulse count of approximately 10 achieves 85% of the maximum data margin. The pulse count may vary for different cells. However, it is desirable to achieve a data margin of at least 85% of the maximum data margin.

In 806, the pulse width that meets the target programming time is determined. For example, assuming "program verify" takes 5 microseconds and the two volt ("V2") program distribution is programmed in 5 microseconds, the middle program distributions will be programmed with 7.5 microseconds pulse width.

Programming Time = pulse count x (pulse width + verify time) Eqn. 3

Programming Time for V0 = 10 x (7.5μs + 5μs)
= 125us

Programming Time for V1 = 10 x (7.5μS + 5μs)
= 125us

Programming Time for V2 = 5 x (5μs +5μs)
= 50μs

Total time = Time for V0 + Time for V1 + Time for V2 Eqn. 4
= 125μs + 125μs + 50μs
= 300μs

V0 is the zero volt program distribution, V1 is the one volt program distribution, and V2 is the two volt program distribution.

In 808, the program voltage that will complete the V0 program distribution in the allocated number of pulses is determined.

In 810, the cells to be programmed at V1 is programmed with the same pulse count as V0 using a predetermined voltage offset to the V0 program voltage. An analysis of the cell can determine this offset. The offset is constant from cell to cell regardless of number of cycles the cell has been used and fabrication variations between lots. Thus, a cell with faster programming at 17.5V requires the same offset as a cell with slower programming that has a V0 program voltage of 18.5V.

Program Voltage (V1) = Program voltage (V0) + offset Eqn. 5

= 18.0V + 1.0V

= 19.0V

In 812, the cells to be programmed at V2 are programmed with as few pulses as possible to minimize programming time. For example, 5 pulses. As shown in Figure 7, the program distribution 702 represents V1 and the curves 704 and 706 represent V2 programmed with 10 and 5 pulses, respectively. Since the program margin, 708 to 710, is the same for both program distributions 704 and 706, program distribution 706 is used because it is programmed with only 5 pulses. The width of the V2 program distribution of V2 is not critical because no voltage distribution exist above the V2.

Traditionally, an array of cells is programmed sequentially regardless of the value to be programmed. In order to improve programming time, the order of programming is changed. All cells in the memory (array, page, or group) are set to the erase state, then all cells in the memory that are to be programmed with V2 are programmed first. By programming V2 first, the programming with the fewest number of pulses prevents this less accurate programming from interfering with the programming of VT0 and VT1. Then all the cells to be programmed with V1 are programmed with an initial voltage and the determined number of pulses. Finally, the cells to be programmed with V0 are programmed with the initial voltage plus an offset and the determined number of pulses. The order of programming V1 and V0 can be reversed as desired. This method of programming mulit-level cells maintains at least 85% of the data margin and greatly reduces the programming time.

Figure 9, is a diagram of an embodiment of a memory 900 with memory cells 902, a pulse count determinator 904, a programming voltage determinator 906, and a cell programmer 908. The memory cells 902 preferably include a plurality of pages of multi-bit cells. The pulse count determinator 904 determines the pulse counts required for programming the cells. The programming voltage determinator 906 determines the programming voltages required to program the cells. The cell programmer 908 can include an erase circuit and a cell programmer circuit. The erase circuit erases a particular cell, or preferably erases a page of cells.

While preferred embodiments have been shown and described, it will be understood that they are not intended to limit the disclosure, but rather it is intended to cover all modifications and alternative methods and apparatuses falling within the spirit and scope of the invention as defined in the appended claims or their equivalents.

WHAT IS CLAIMED IS:

1. A method of programming a plurality of multi-level memory cells 902 within a programming time target, the multi-level memory cells 902 having at least first, second, third and fourth programming levels, the fourth programming level being the erase state, the first programming level being the programming level furthest from the fourth programming level, the second and third programming levels being within the first and fourth programming levels, comprising:
erasing the plurality of multi-level memory cells 902;
programming a first group of multi-level memory cells 902 with the first programming level with a first programming pulse count, a first pulse width, and a first programming voltage;
programming a second group of multi-level memory cells 902 with the second programming level with a second programming pulse count, a second pulse, width and a second programming voltage; and
programming a third group of multi-level memory cells 902 with the third programming level with a third programming pulse count, a third pulse width, and a third programming voltage.

2. The method of claim 1, wherein the plurality of multi-level memory cells 902 comprises a page of multi-level NAND memory cells 902.

3. The method of claim 1, wherein the cells are multi-level flash memory cells 902.

4. The method of claim 1, wherein the first programming pulse count is the minimum pulse count required to program the cell.

5. The method of claim 1, wherein the second programming pulse count is selected to maintain at least 85% of the maximum programming margin.

6. A memory device 900, characterized in that a plurality of memory cells 902, a pulse count determination means 904, a program voltage determination means 906, and a cell programming means 908 program the memory device 900 such that the memory cells 902 are programmed with a voltage level from the group of a first, second, third, and fourth voltage levels, where each voltage level corresponds to a plurality of bits of information, the plurality of memory cells 902 comprises a first, second, third, and fourth group of cells 902; the pulse count determination means 904 determines first, second, and third pulse counts for programming the first, second, and third group of cells 902, respectively; the program voltage determination means 906 determines the first, second, and third program voltages for programming the first, second, and third group of cells 902, respectively; and the cell programming means 908 programs each of the plurality of cells 902 with a voltage level from the group of first, second, third, and four voltage levels, the cell programming means 908 programming the plurality of memory cells 902 with the fourth voltage level, then programming the first group of cells 902 to the first voltage level using the first program voltage and the first pulse count, then programming the second group of cells 902 to the second voltage level using the second program voltage and the second pulse count, then programming the third group of cells 904 to the third voltage level using the third program voltage and the third pulse count.

7. A memory device 900, comprising:

(a) a plurality of memory cells 902 capable of being programmed with a first, second, third, and fourth voltage levels, each voltage level corresponding to a plurality of bits of information, the plurality of memory cells 902 including a first, second, third, and fourth group of cells 902;

(b) a pulse count determinator 904 capable of determining a first, second, and third pulse counts for programming the first, second, and third group of cells 902, respectively;

(c) a program voltage determinator 906 being capable of determining a first, second, and third program voltages for programming the first, second, and third group of cells 902, respectively; and

(d) a cell programmer 908 capable of programming each of the plurality of cells 902 in the plurality of memory cells 902 with the first, second, third, and four voltage levels, the cell programmer 908 programming the plurality of memory cells 902 with the fourth voltage level, then programming the first group of cells 902 to the first voltage level using the first program voltage and the first pulse count, then programming the second group of cells 902 to the second voltage level using the second program voltage and the second pulse count, then programming the third group of cells 902 to the third voltage level using the third program voltage and the third pulse count.

8. The memory device 900 of claim 7, wherein the fourth voltage level is the erase voltage level.

9. The memory device 900 of claim 7, wherein the cell programmer 908 includes a cell erase circuit 908 and a cell programming circuit 908, the cell erase circuit 908 being capable of erasing one or more of the plurality of cells, the cell programming circuit 908 being capable of programming one or more of the plurality of cells 902 to the first, second, and third voltage levels.

10. The memory device 900 of claim 7, wherein the second pulse width is selected such that the combination of the programming times for the first, second, and third programming levels is within the programming time target.

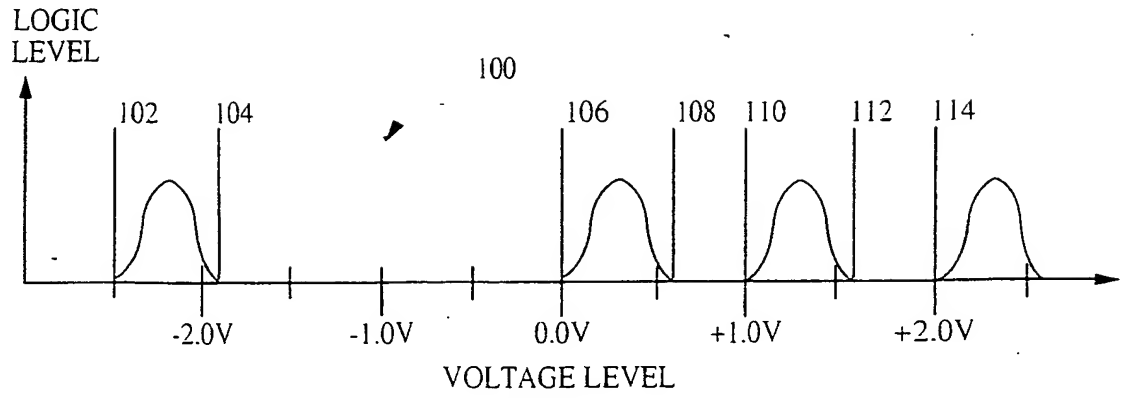


FIG. 1
PRIOR ART

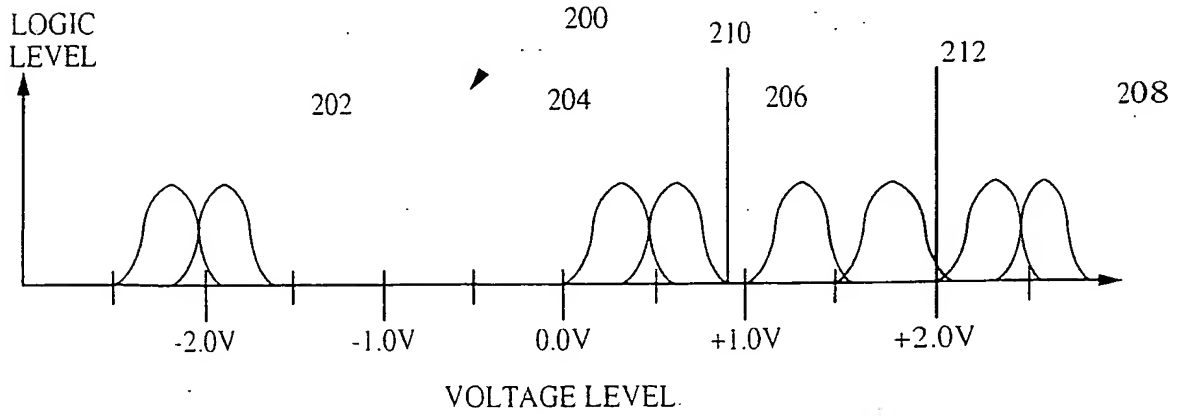


FIG. 2
PRIOR ART

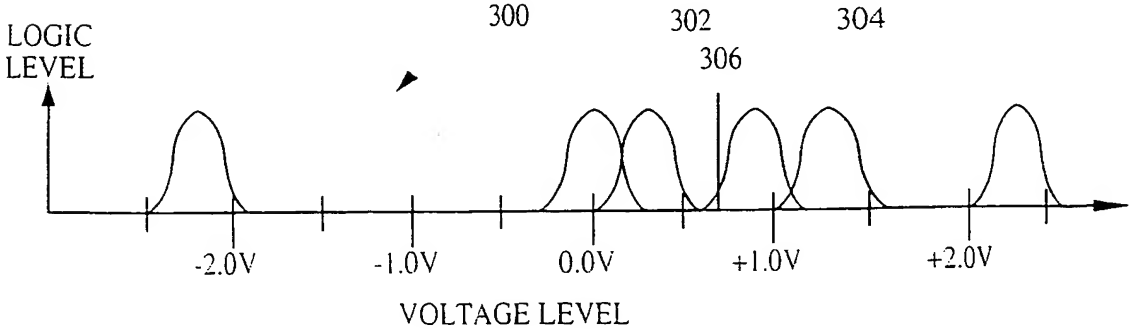
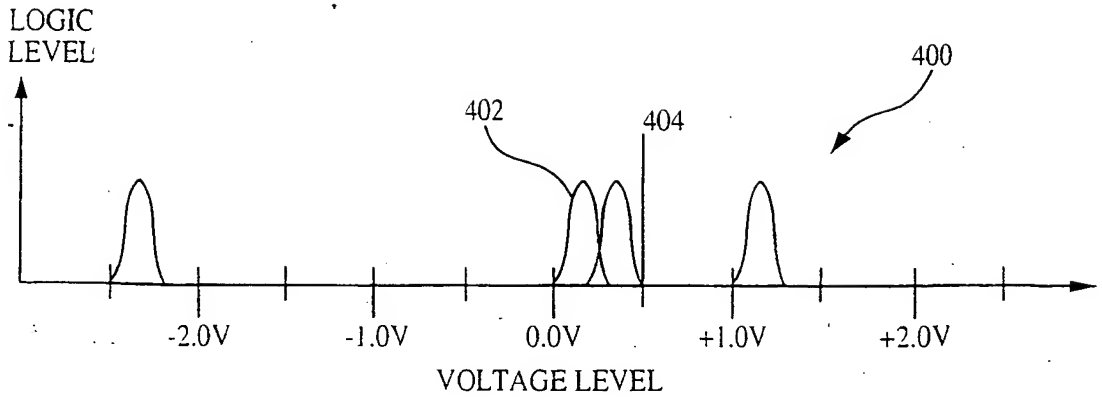


FIG. 3
PRIOR ART


LOGIC
LEVEL
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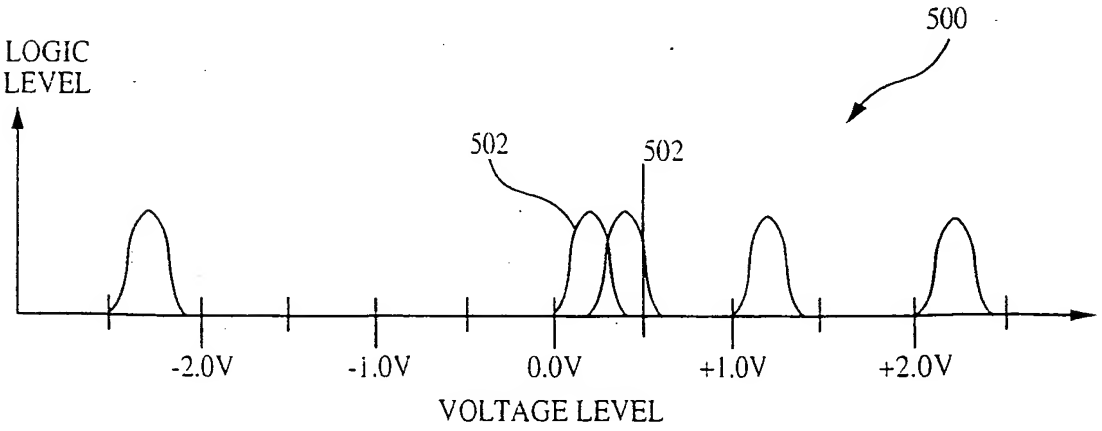
402
404
-2.0V
-1.0V
0.0V
+1.0V
+2.0V
VOLTAGE LEVEL

FIG. 4


500
LOGIC
LEVEL
502
502
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-1.0V
0.0V
+1.0V
+2.0V
VOLTAGE LEVEL

FIG. 5

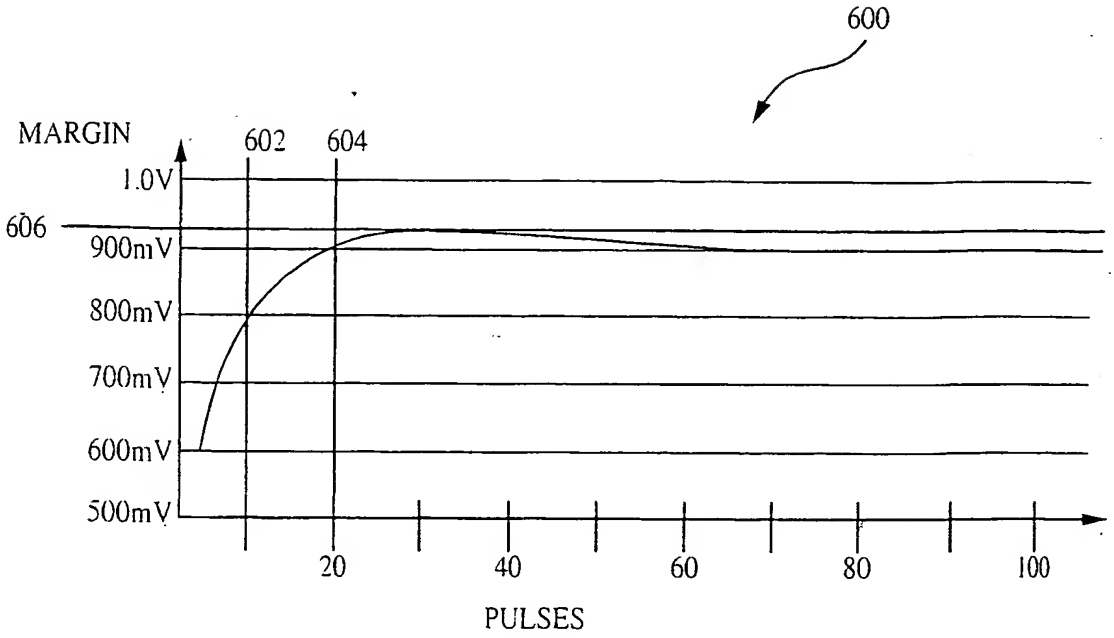
600
MARGIN
602
604
1.0V
606
900mV
800mV
700mV
600mV
500mV
20
40
60
80
100
PULSES

FIG. 6

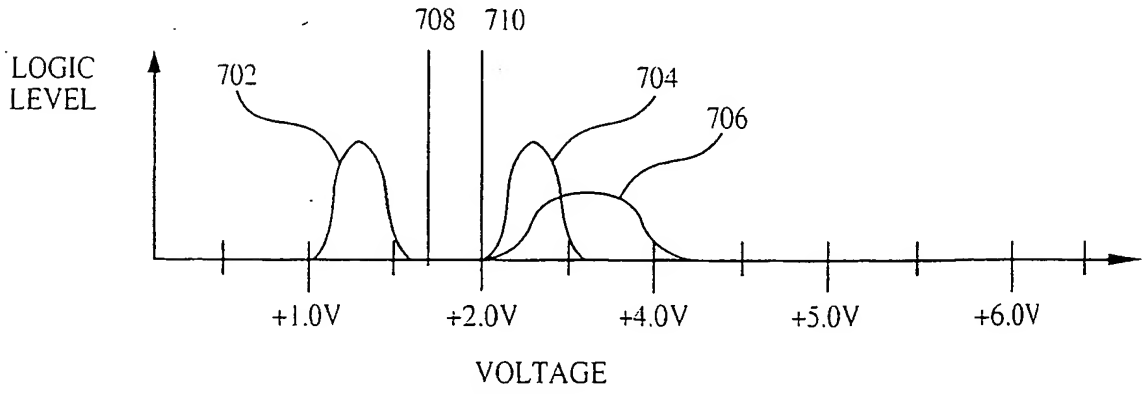
708
710
LOGIC LEVEL
702
704
706
+1.0V
+2.0V
+4.0V
+5.0V
+6.0V
VOLTAGE

FIG. 7

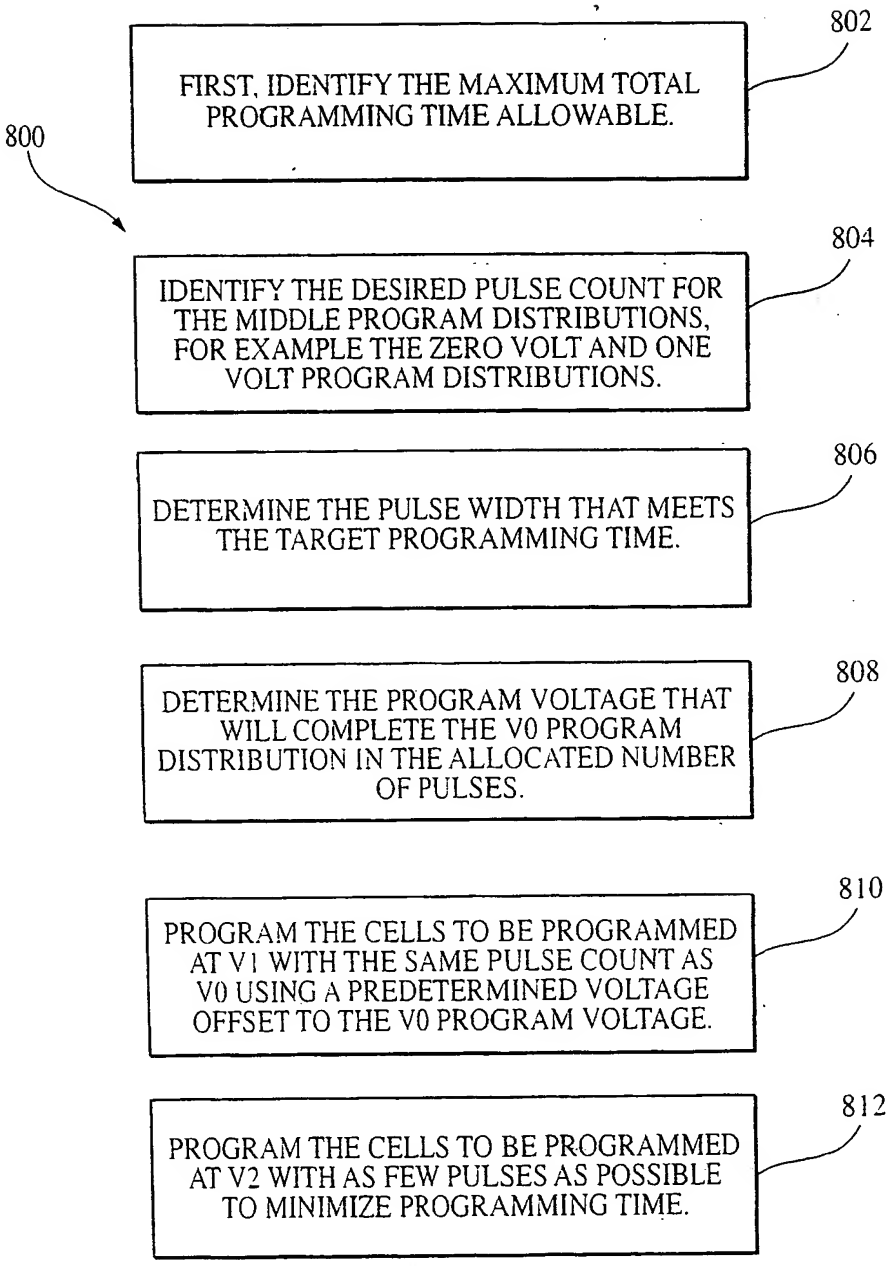
800
802
FIRST, IDENTIFY THE MAXIMUM TOTAL PROGRAMMING TIME ALLOWABLE.
804
IDENTIFY THE DESIRED PULSE COUNT FOR THE MIDDLE PROGRAM DISTRIBUTIONS, FOR EXAMPLE THE ZERO VOLT AND ONE VOLT PROGRAM DISTRIBUTIONS.
806
DETERMINE THE PULSE WIDTH THAT MEETS THE TARGET PROGRAMMING TIME.
808
DETERMINE THE PROGRAM VOLTAGE THAT WILL COMPLETE THE V0 PROGRAM DISTRIBUTION IN THE ALLOCATED NUMBER OF PULSES.
810
PROGRAM THE CELLS TO BE PROGRAMMED AT V1 WITH THE SAME PULSE COUNT AS V0 USING A PREDETERMINED VOLTAGE OFFSET TO THE V0 PROGRAM VOLTAGE.
812
PROGRAM THE CELLS TO BE PROGRAMMED AT V2 WITH AS FEW PULSES AS POSSIBLE TO MINIMIZE PROGRAMMING TIME.

FIG. 8

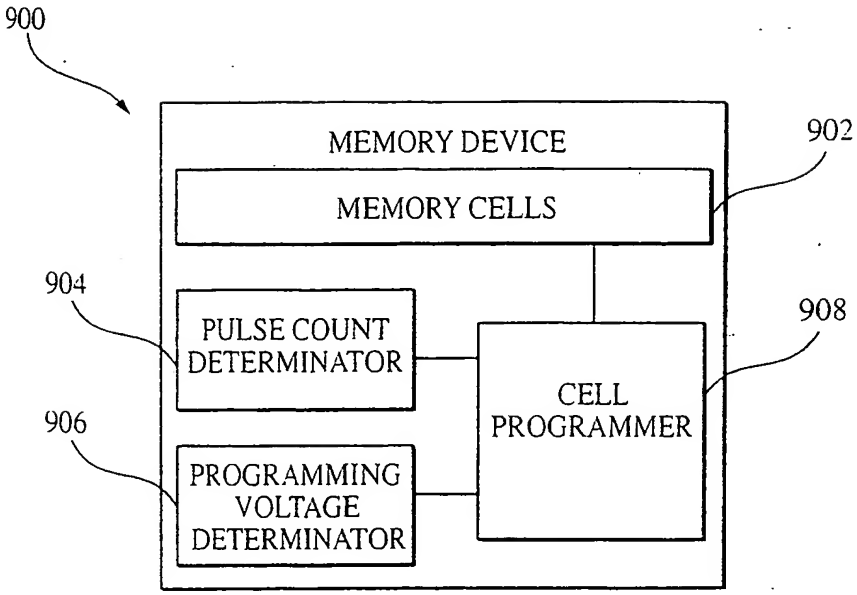
900
MEMORY DEVICE
902
MEMORY CELLS
904
PULSE COUNT DETERMINATOR
908
CELL PROGRAMMER
906
PROGRAMMING VOLTAGE DETERMINATOR

FIG. 9

INTERNATIONAL SEARCH REPORT

Internatic * Application No
PCT/US 01/03857

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 G11C11/56

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 G11C

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data, PAJ, INSPEC

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 5 959 882 A (KUBONO SHOOJI ET AL) 28 September 1999 (1999-09-28) column 7, line 43 -column 8, line 60 figure 1	1,3-10
Y	US 5 801 989 A (KIM JIN-KI ET AL) 1 September 1998 (1998-09-01) column 3, line 23 - line 39	1,3-10
A	EP 0 969 478 A (SHARP KK) 5 January 2000 (2000-01-05) page 2, line 13 - line 25	1,6,7
A	US 5 768 188 A (SUH KANG-DEOG ET AL) 16 June 1998 (1998-06-16) column 8, line 9 -column 9, line 28 figures 1-3	2

☐ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

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Date of the actual completion of the international search	Date of mailing of the international search repon
22 May 2001	29/05/2001

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Colling, P

INTERNATIONAL SEARCH REPORT

Internatic Application No
PCT/US 01/03857

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 5959882 A	28-09-1999	JP 3062730 B	12-07-2000
		JP 10027486 A	27-01-1998
		TW 381224 B	01-02-2000
US 5801989 A	01-09-1998	KR 185611 B	15-04-1999
		JP 9180481 A	11-07-1997
		TW 391008 B	21-05-2000
EP 0969478 A	05-01-2000	JP 2000021185 A	21-01-2000
		US 6172912 B	09-01-2001
US 5768188 A	16-06-1998	KR 172408 B	30-03-1999
		JP 9180472 A	11-07-1997